

iM8XM LPDDR4 Board Analysis using SIPro and Memory Designer

Keysight Technologies

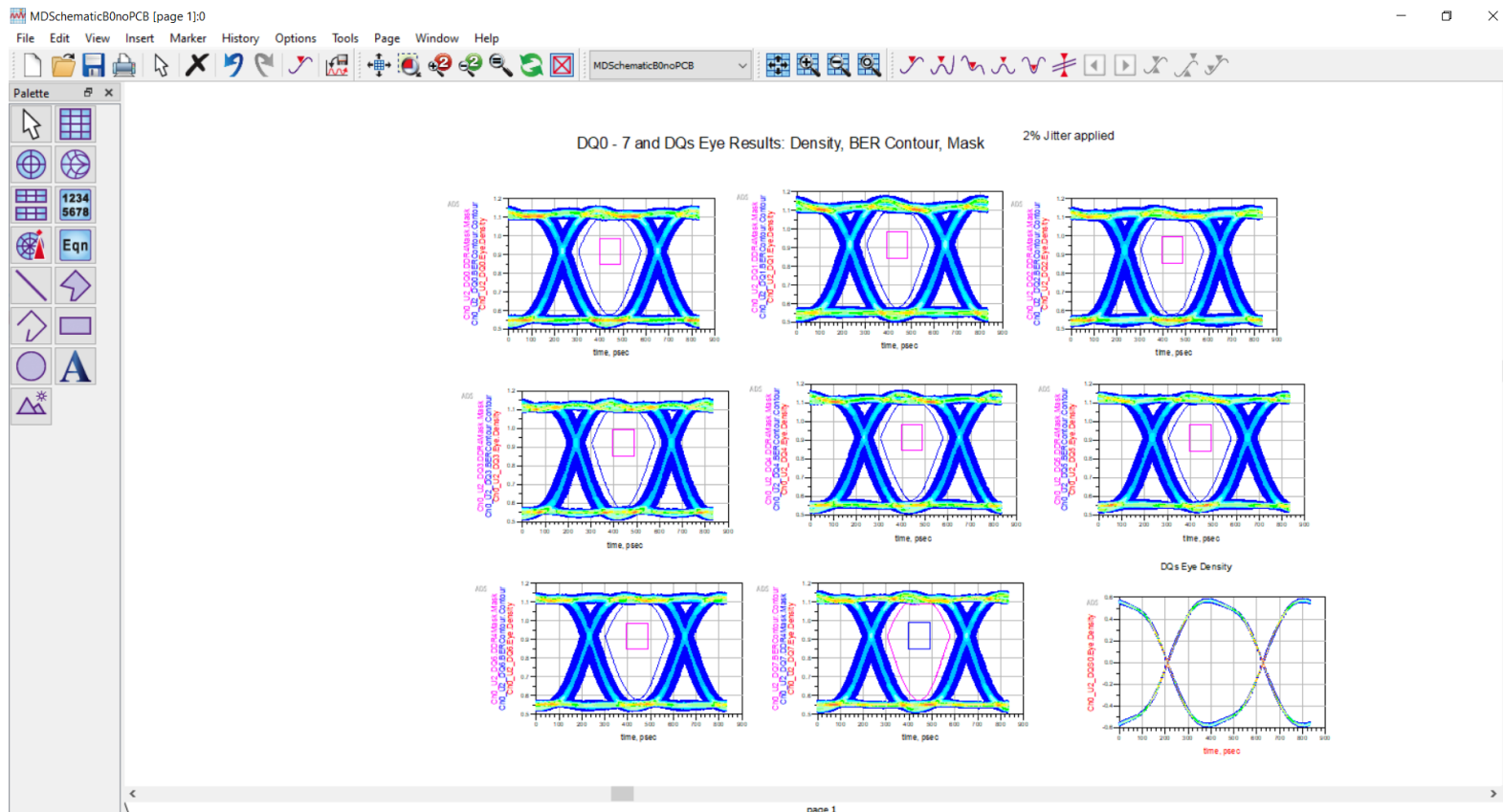
11/15/2021



Overview for Today

END GOAL: OBSERVE THE EYE RESULTS

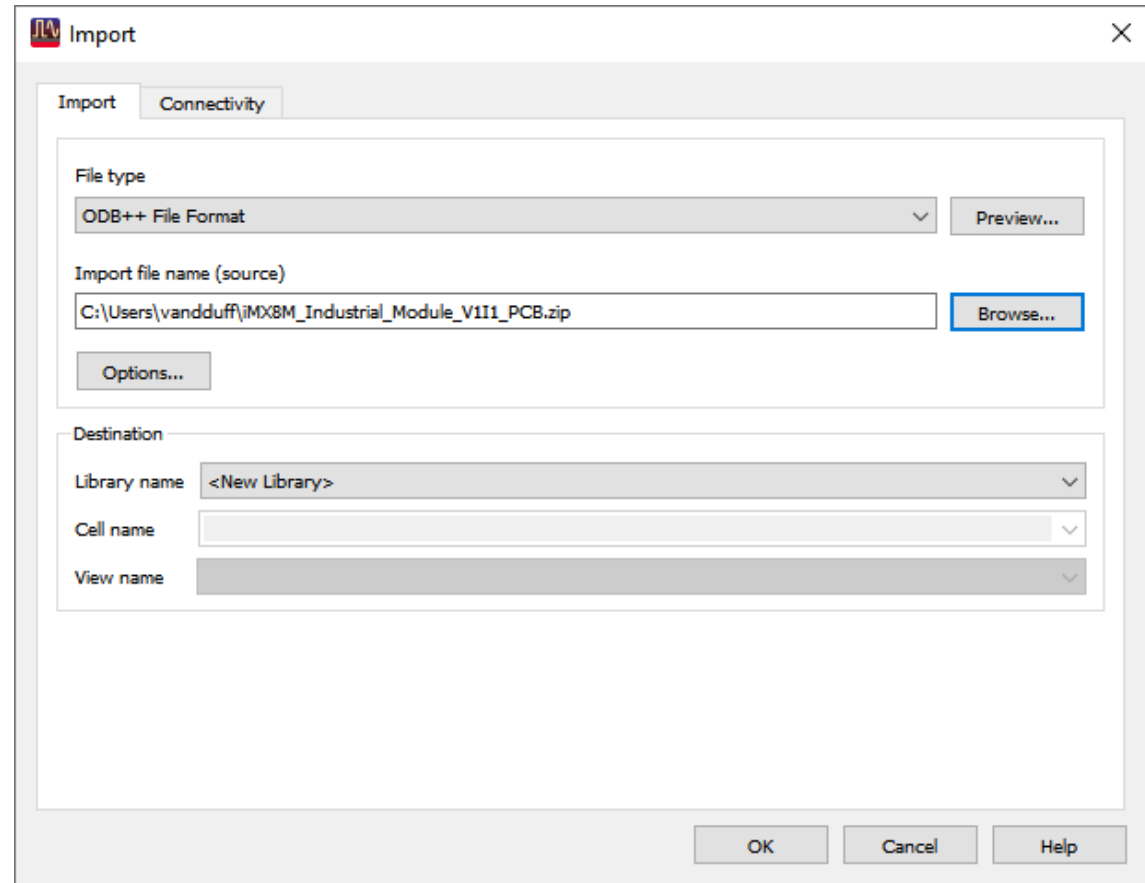
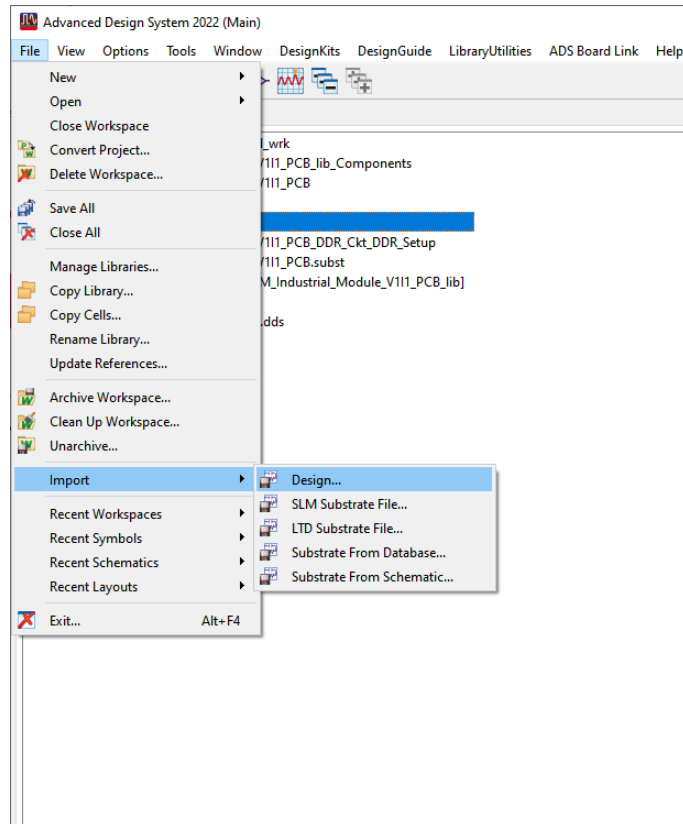
- Byte 0 of Channel A Eye Results with 2% Jitter applied



Overview for Today

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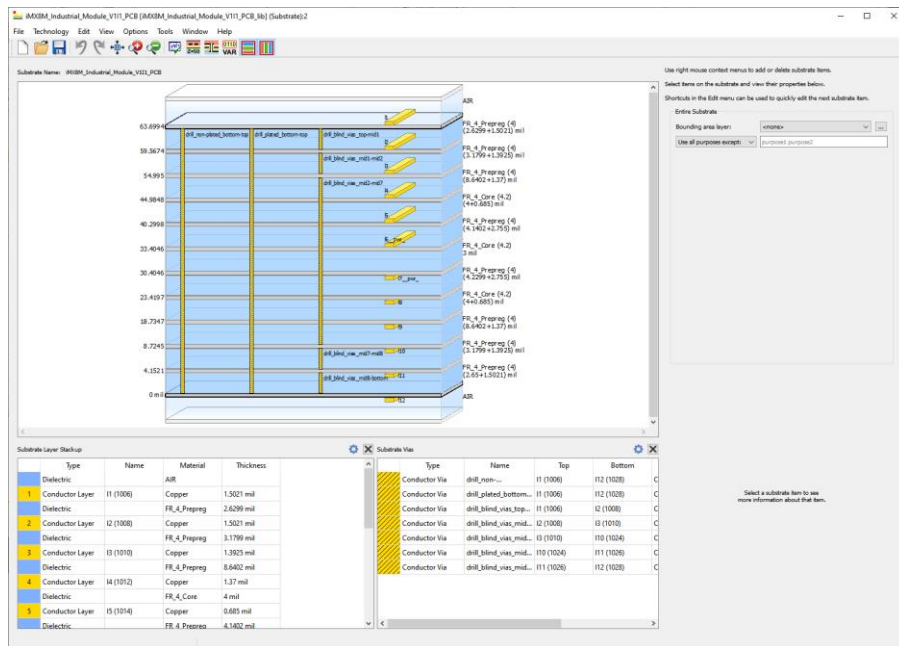
- Import board into ADS using ODB++ file type:



Overview for Today

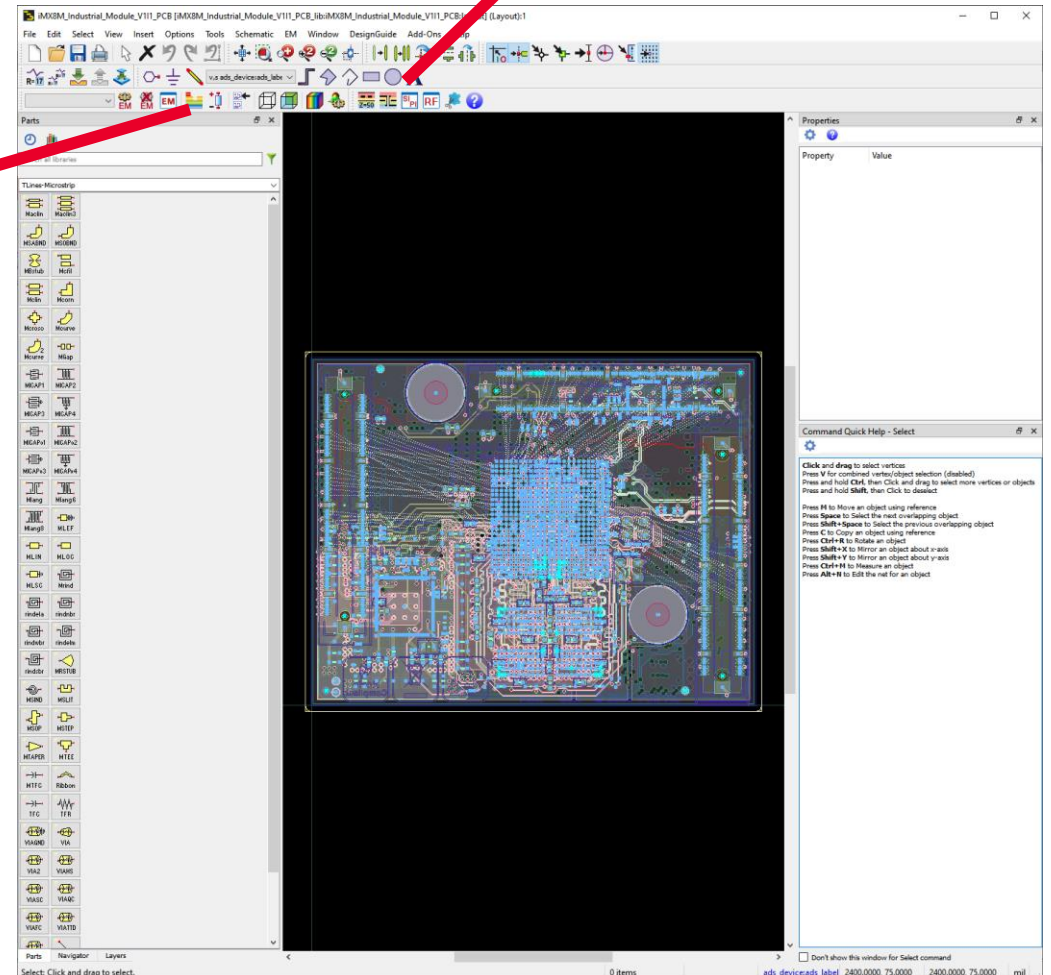
END GOAL: OBSERVE THE EYE RESULTS

- Board has been imported and now we observe the board in layout:



Substrate editor

Next: Launch SIPro for Analysis



Board in layout

Analysis of Channel A DQ Signals and DQs

END GOAL: OBSERVE THE EYE RESULTS

- Run RapidScan Z0 Tool to check:
 - Substrate stackup is setup correctly
 - View sections of the net
 - Characteristic impedance falls within x% of initial design

The screenshot displays the Altium Designer interface. The main window shows a PCB layout with components U1, U2, and U3. A context menu is open over the layout, with 'RapidScan Z0' selected. In the foreground, the 'Net Analysis Result (netAnalysis 5)' window is open, showing a table of net analysis results and a detailed view of sections for net DRAM_DATA3_A.

Net Name	Start Pin	End Pin	Total Delay [ps]	Z0 (longest section)	Length [mil]	Width [mil]	Layer	Via Count
DRAM_DATA0_A	U1.AE23	U2.E2	114.3	39.9	510.1	5.1	I3 (1010)	4
DRAM_DATA1_A	U1.AD04	U2.C2	107.0	39.9	525.0	5.1	I3 (1010)	4
DRAM_DATA2_A	U1.AE22	U2.E2	125.8	39.9	640.2	5.1	I3 (1010)	4
DRAM_DATA3_A	U1.AD22	U2.F2	119.7	39.9	612.3	5.1	I3 (1010)	4
DRAM_DATA4_A	U1.AA24	U2.F4	107.2	39.9	537.4	5.1	I3 (1010)	4
DRAM_DATA5_A	U1.V25	U2.E4	108.8	39.9	542.0	5.1	I3 (1010)	4
DRAM_DATA6_A	U1.AA25	U2.C4	115.3	39.9	575.0	5.1	I3 (1010)	4
DRAM_DATA7_A	U1.AB25	U2.B4	115.7	39.9	548.8	5.1	I3 (1010)	4
DRAM_DATA8_A	U1.AB22	U2.B11	203.7	39.9	853.0	5.1	I10 (1024)	2
DRAM_DATA9_A	U1.AA22	U2.C11	201.2	39.9	864.1	5.1	I10 (1024)	2
DRAM_DATA10_A	U1.AA23	U2.E11	196.6	39.9	875.2	5.1	I10 (1024)	2
DRAM_DATA11_A	U1.AA20	U2.F11	206.9	39.9	937.0	5.1	I10 (1024)	2
DRAM_DATA12_A	U1.AA18	U2.F9	205.8	39.9	928.0	5.1	I10 (1024)	2
DRAM_DATA13_A	U1.AB19	U2.E9	205.7	39.9	928.5	5.1	I10 (1024)	2
DRAM_DATA14_A	U1.AA19	U2.C9	215.3	39.9	984.5	5.1	I10 (1024)	2
DRAM_DATA15_A	U1.AA17	U2.B9	210.4	39.9	955.5	5.1	I10 (1024)	2

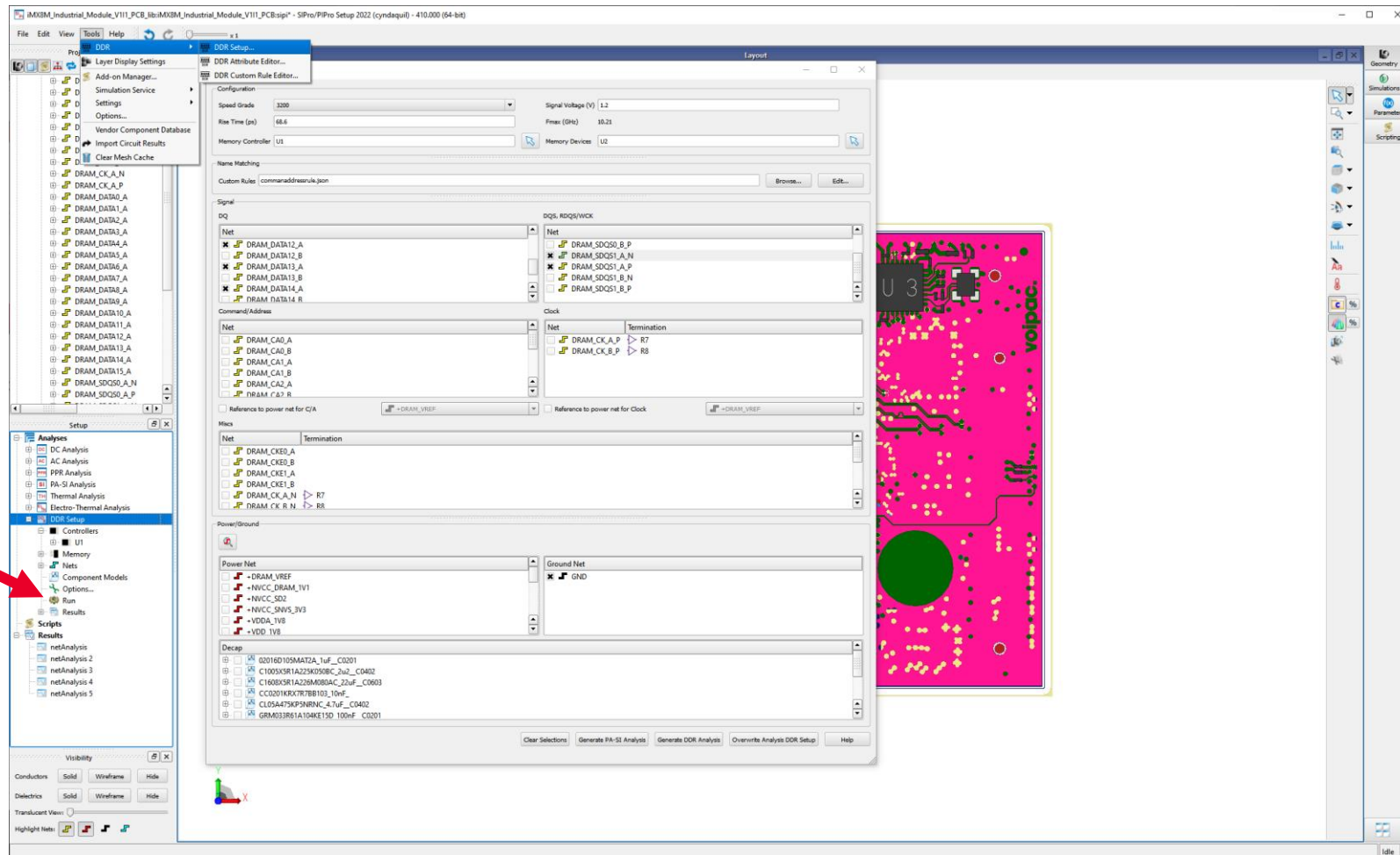
Section	Delay [ps]	Z0 [ohm]	Length [mil]	Width [mil]	Layer	Start [mil]	End [mil]	Return Path	Via Radius [mil]
1 Line	2.9	39.6	19.9	6.8	I1 (1000)	1498.0,710.6	1483.0,724.6	.I2 (1000) [GND]	
2 Via	1.1		4.1			1483.0,724.6	1483.0,724.6		2.0
3 Line	2.9	34.4	17.1	6.1	I2 (1000)	1483.0,724.6	1471.9,736.8	I1 (1000) [GND]	
4 Via	0.8		4.6			1471.9,736.8	1471.9,736.8		2.0
5 Line	103.8	39.9	612.3	5.1	I3 (1010)	1471.9,736.8	1384.3,507.3	I2 (1000) [GND]	
6 Via	1.2		4.6			1384.3,507.3	1384.3,507.3		2.0
7 Line	3.2	37.6	18.9	5.1	I2 (1008)	1384.3,507.3	1396.7,493.1	I1 (1000) [GND]	
8 Via	1.2		4.1			1396.7,493.1	1396.7,493.1		2.0
9 Line	2.6	41.1	18.1	6.4	I1 (1000)	1396.7,493.1	1409.4,480.3	.I2 (1000) [GND]	

Setup DDR Analysis

END GOAL: OBSERVE THE EYE RESULTS

- Set the board up to run DDR analysis of Channel A and corresponding DQs

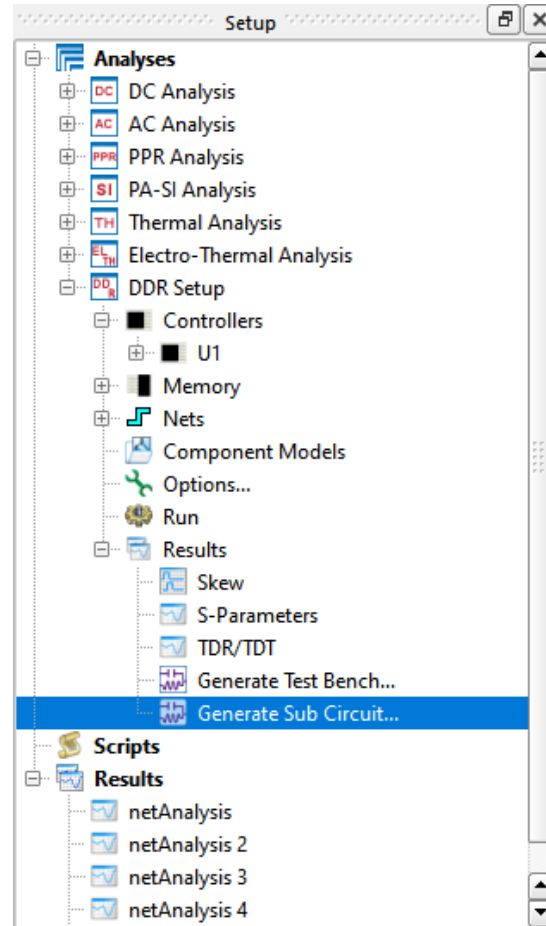
Run
Simulation



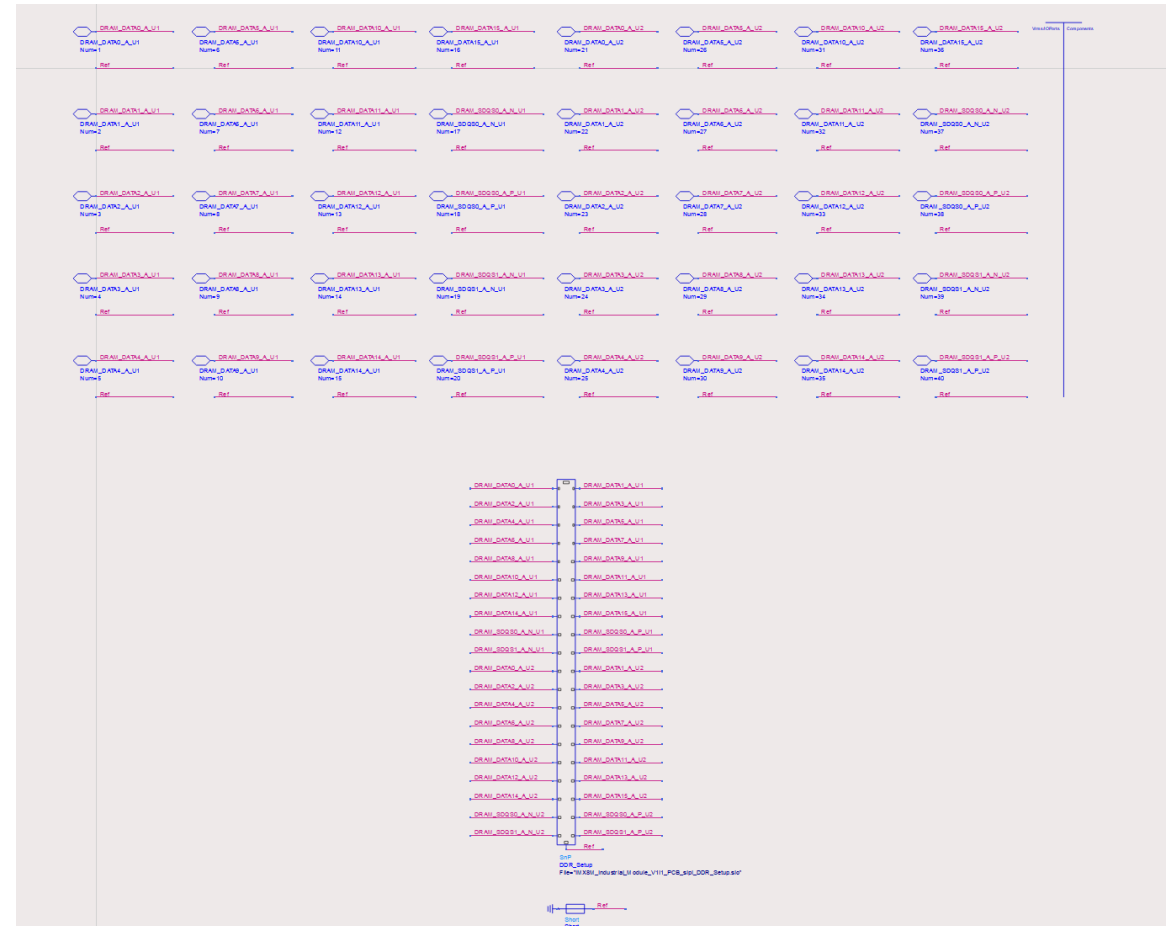
Analyze SIPro DDR Analysis Results

END GOAL: OBSERVE THE EYE RESULTS

- View the results:
 - S-Param insertion loss
 - Skew
 - Utilize sub-circuit to generate info for Memory Designer



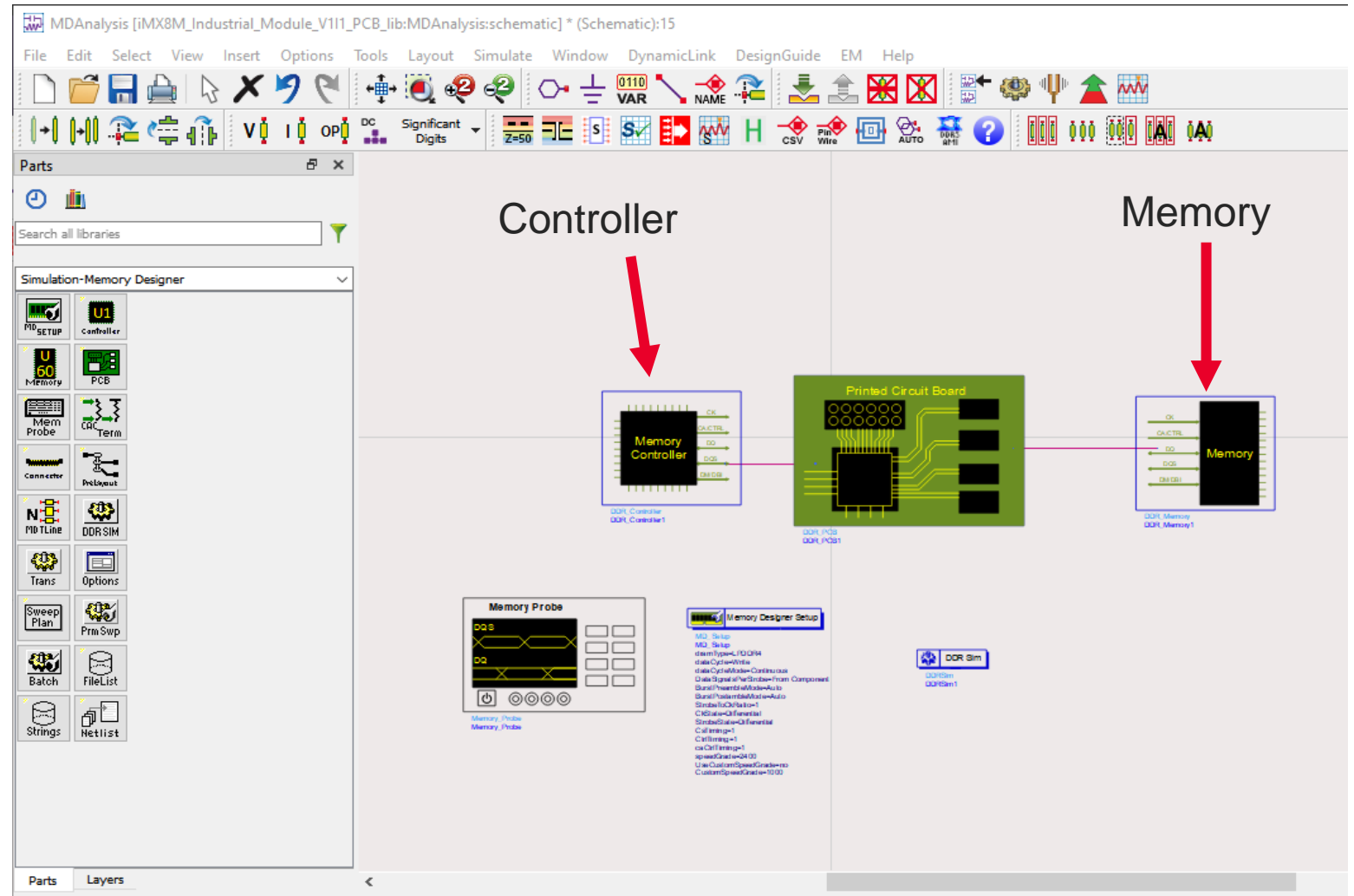
Sub-Circuit Generated:

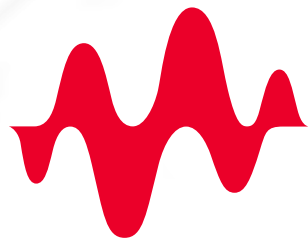


Overview for Today

END GOAL: OBSERVE THE EYE RESULTS

- Memory Designer Setup
- DDR Sim – Which Simulator???
 - Statistical: Takes in ibis analog models(.ibs), good for DDR4 msmts
 - Bit-by-bit: Equalization for Rx model, and IBIS-AMI models, good for DDR5 / LPDDR5
 - Transient Convolution: Takes in S-parameter models to convolve them, giving you waveforms





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