iM8XM LPDDR4 Board Analysis using SIPro and Memory Designer

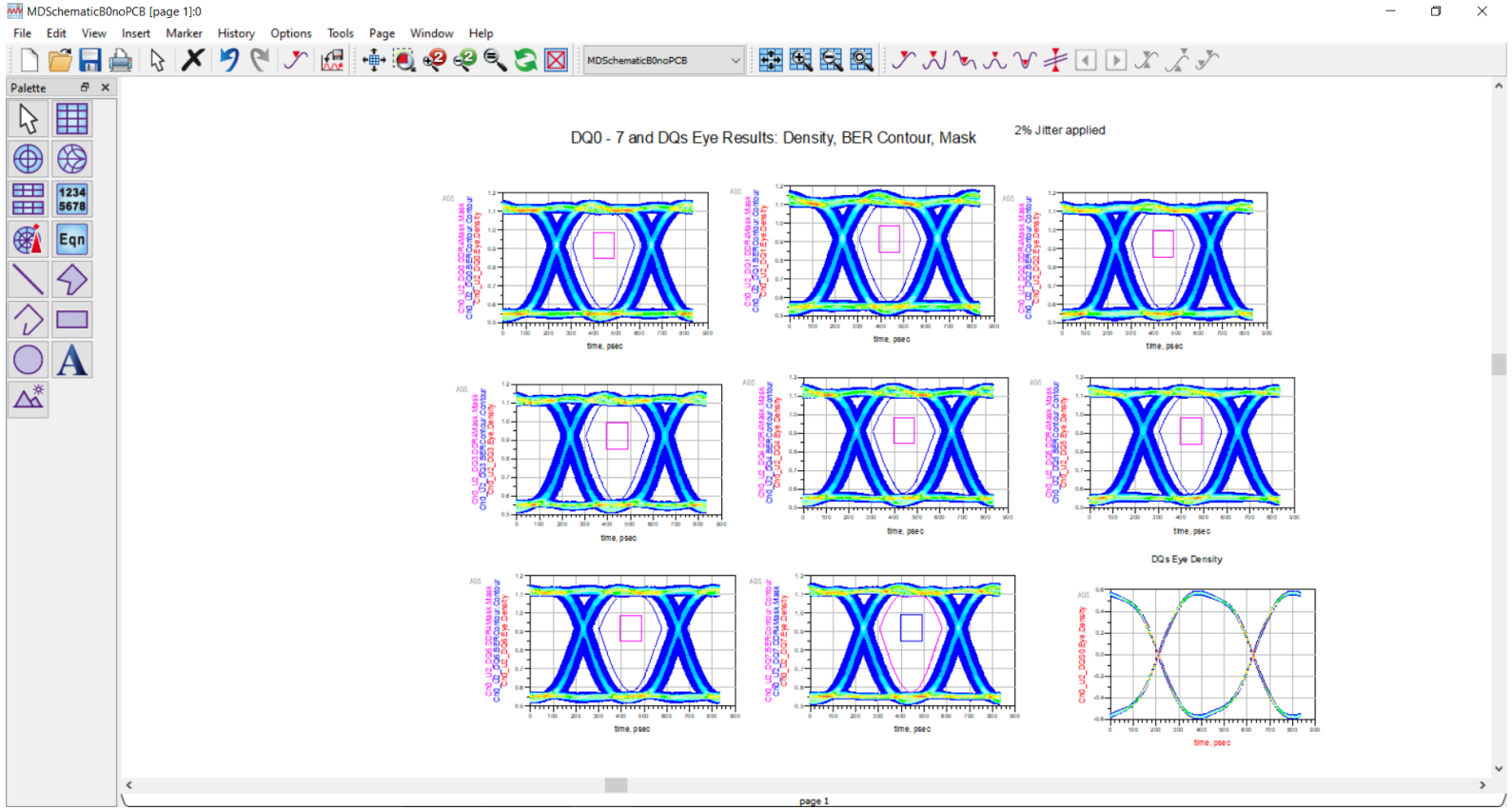
Keysight Technologies | 11/15/2021

KEYSIGHT TECHNOLOGIES

Overview for Today

END GOAL: OBSERVE THE EYE RESULTS

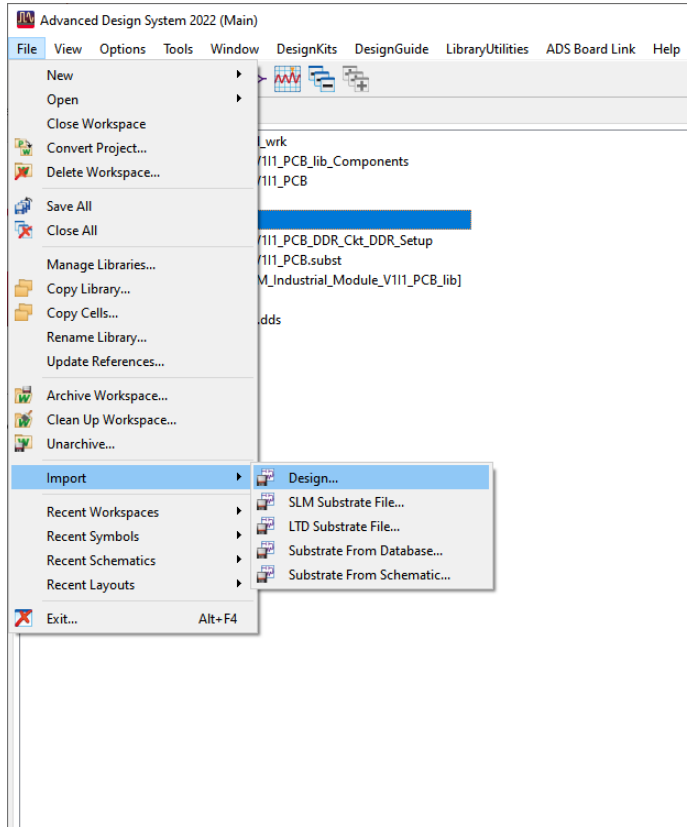
- Byte 0 of Channel A Eye Results with 2% Jitter applied

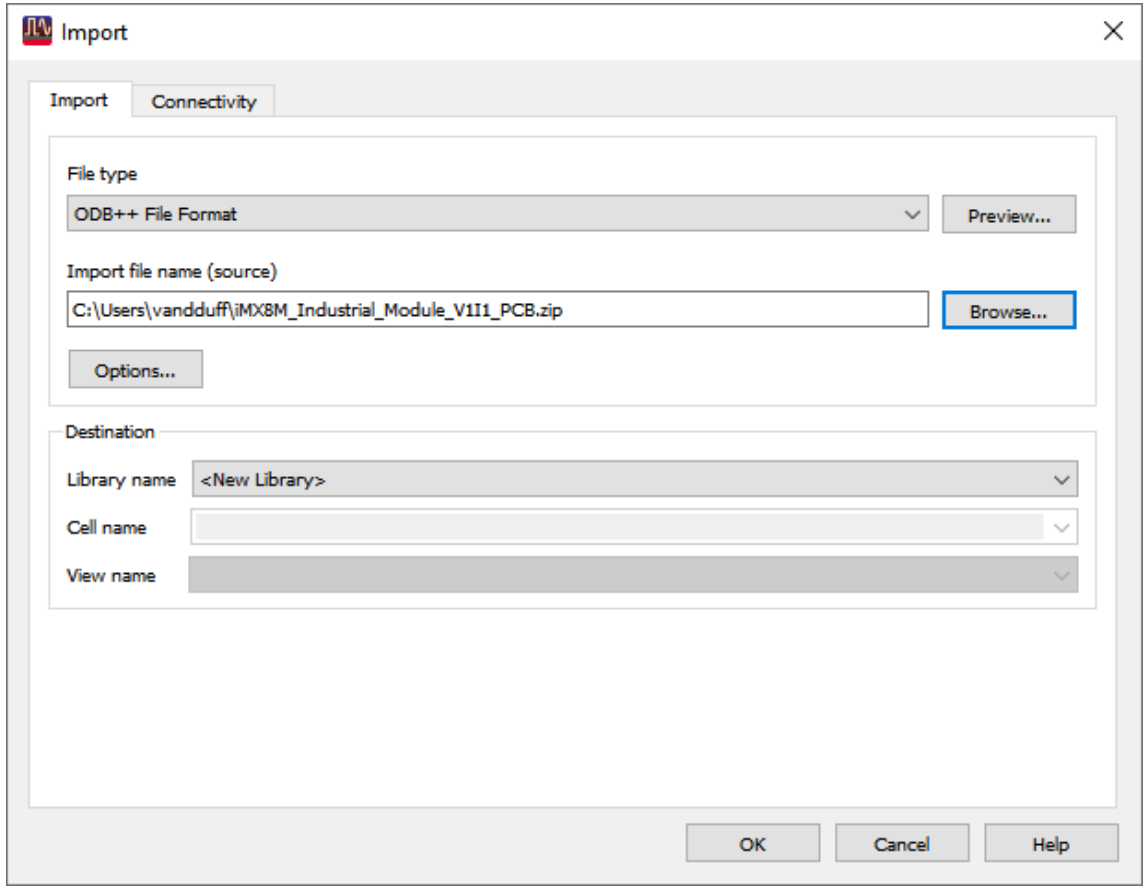


Overview for Today

END GOAL: OBSERVE THE EYE RESULTS

- Import board into ADS using ODB++ file type:



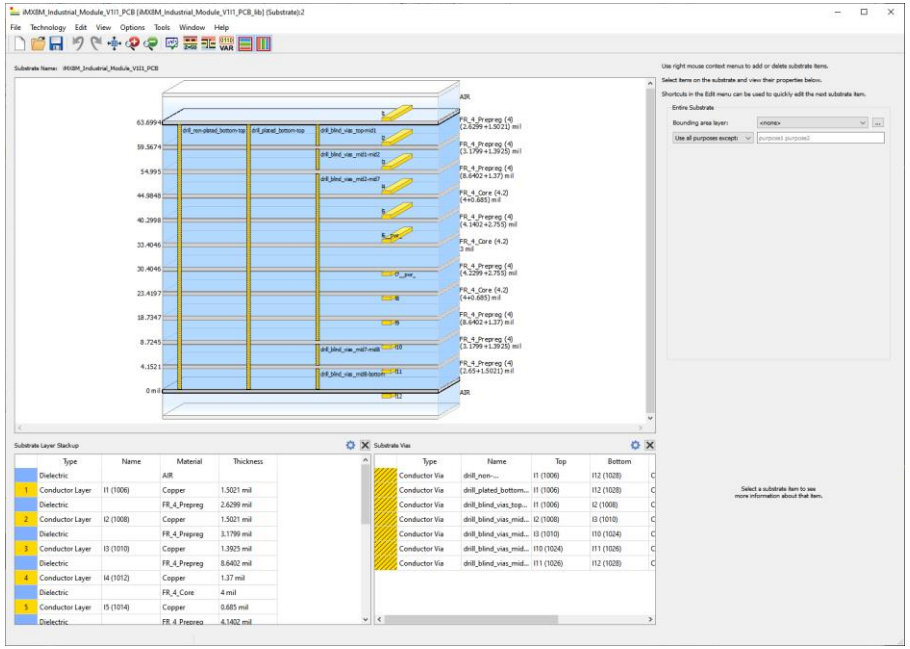


Overview for Today

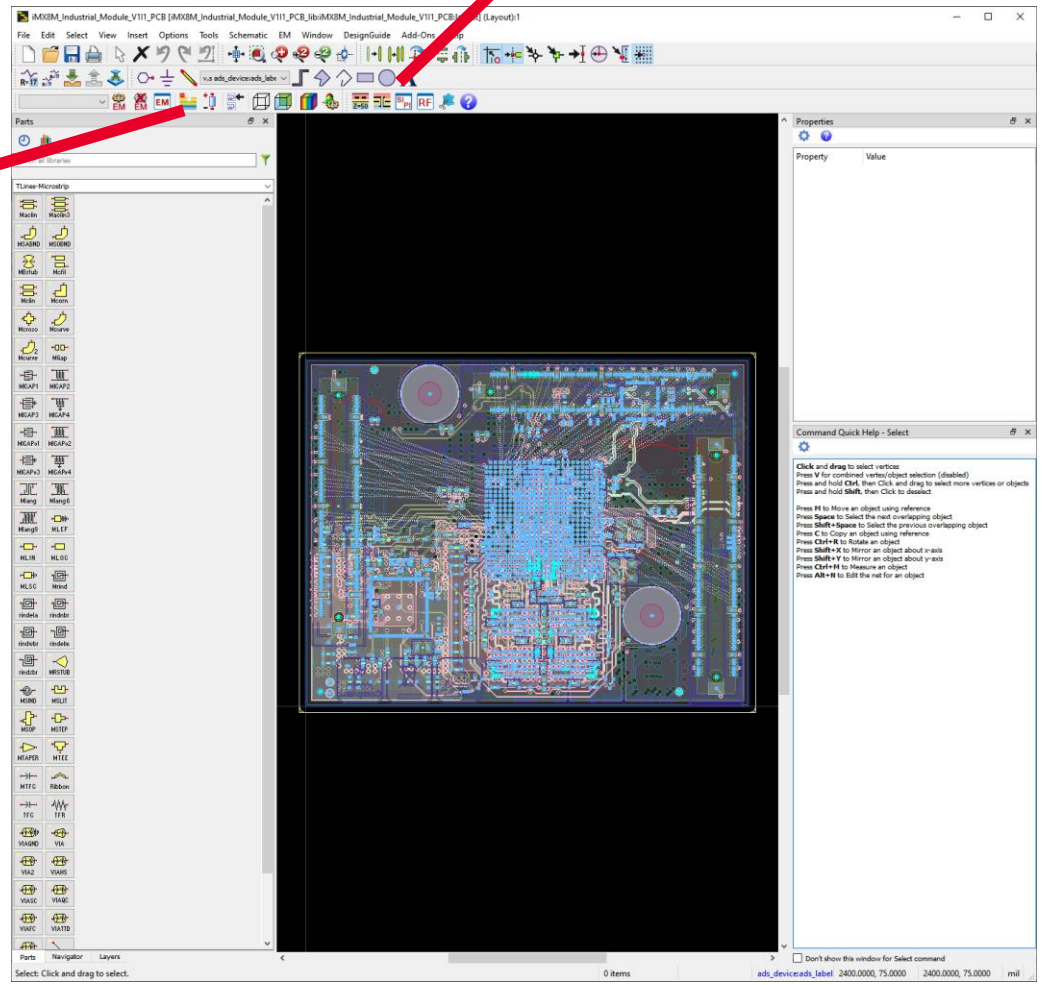
END GOAL: OBSERVE THE EYE RESULTS

Next: Launch SIPro for Analysis

- Board has been imported and now we observe the board in layout:



Substrate editor

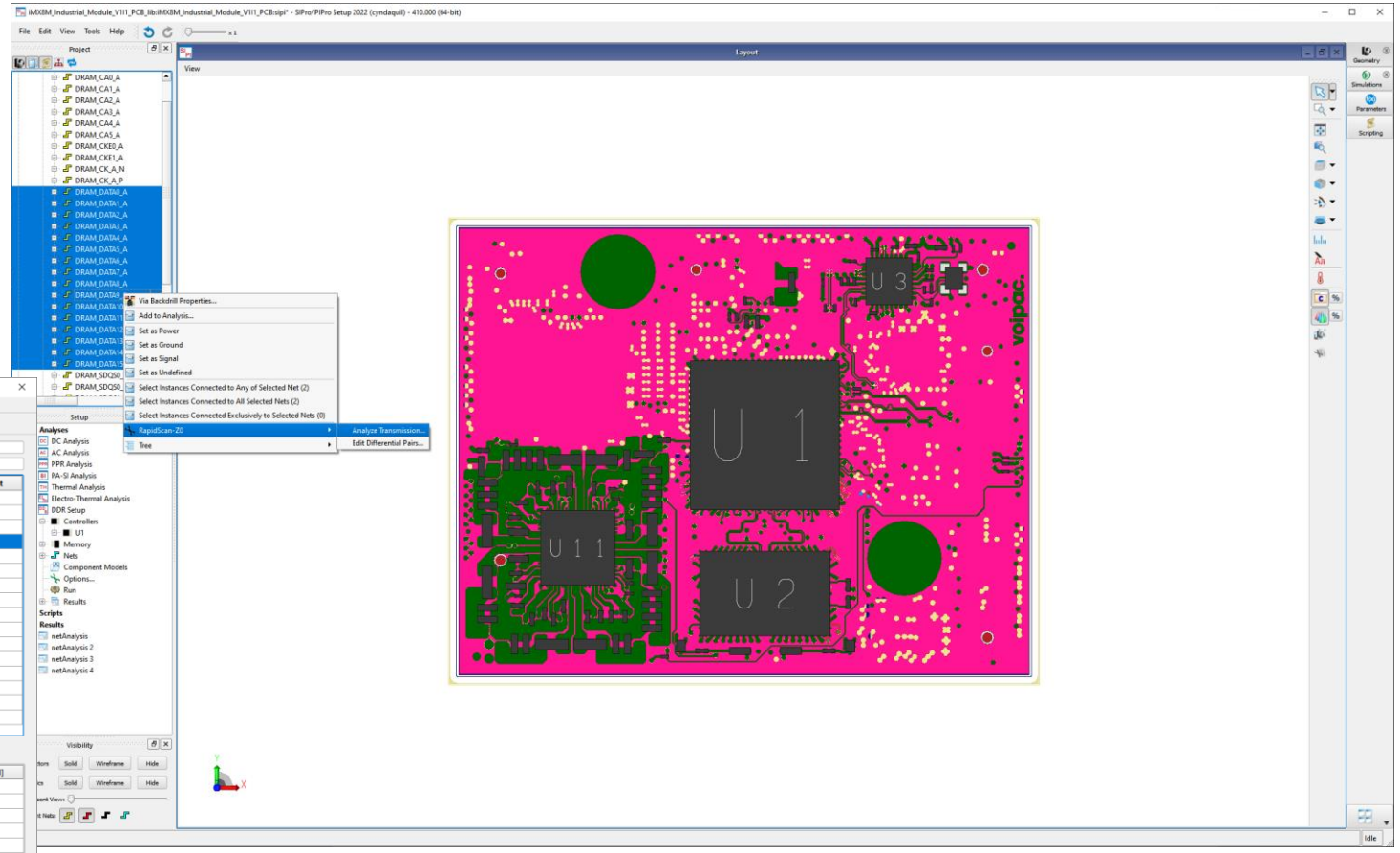


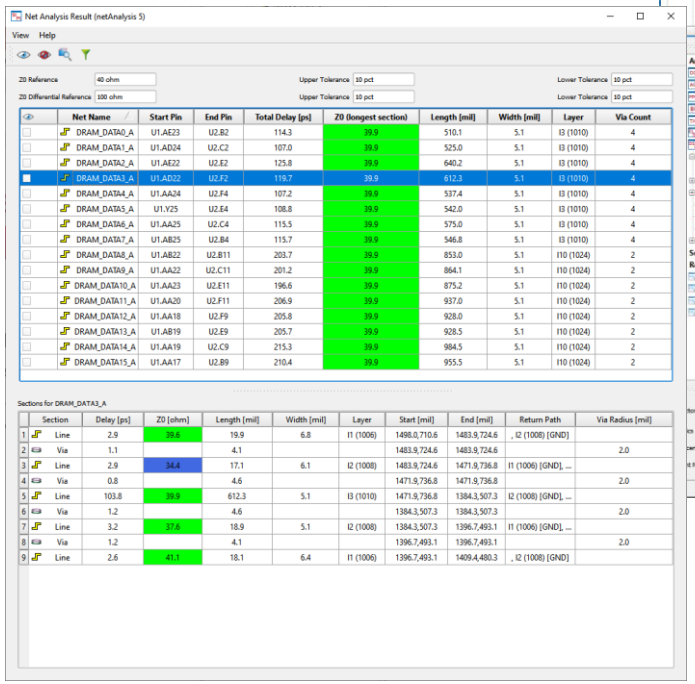
Board in layout

Analysis of Channel A DQ Signals and DQs

END GOAL: OBSERVE THE EYE RESULTS

- Run RapidScan Z0 Tool to check:
  - Substrate stackup is setup correctly
  - View sections of the net
  - Characteristic impedance falls within x% of initial design



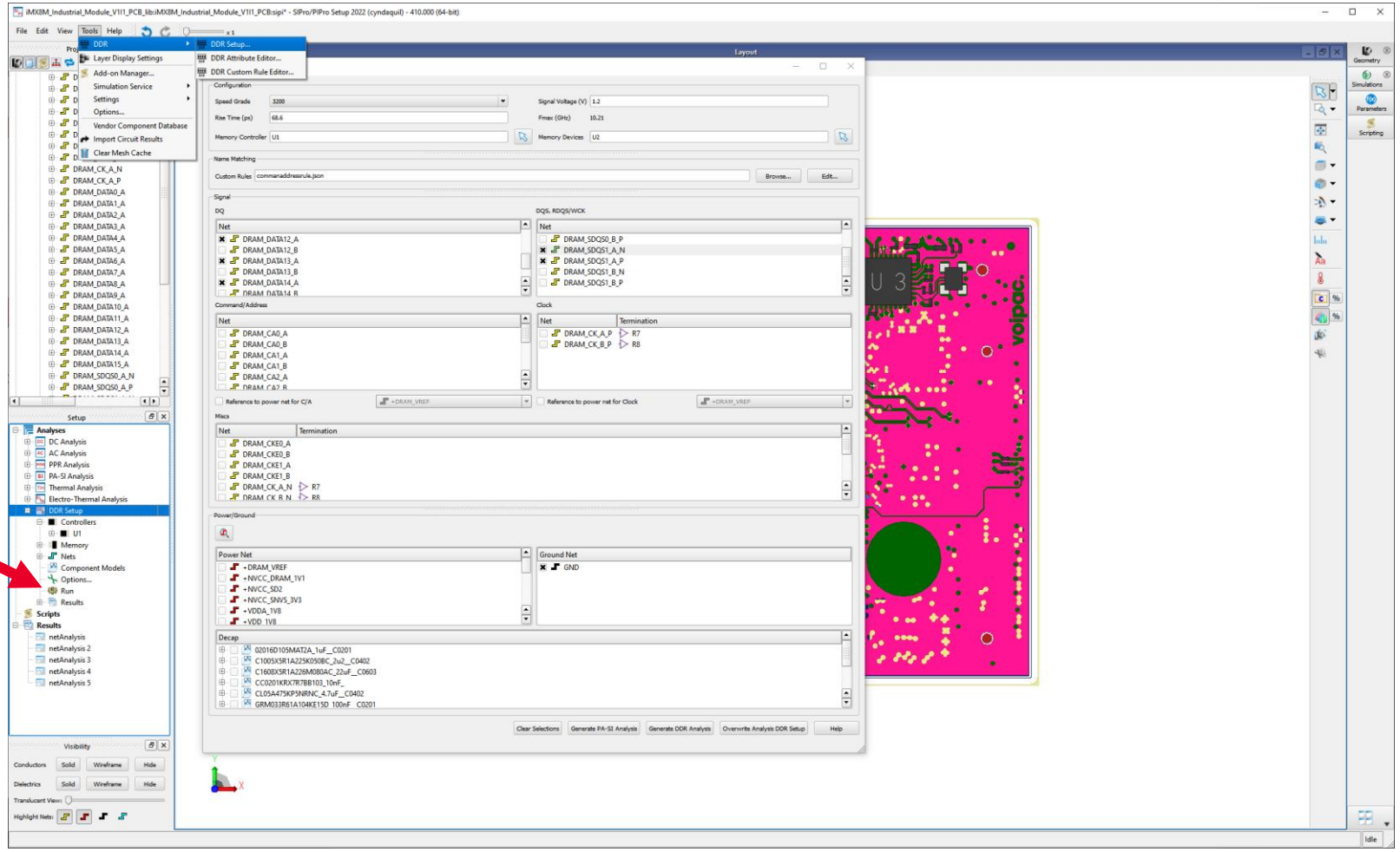


Setup DDR Analysis

END GOAL: OBSERVE THE EYE RESULTS

- Set the board up to run DDR analysis of Channel A and corresponding DQs

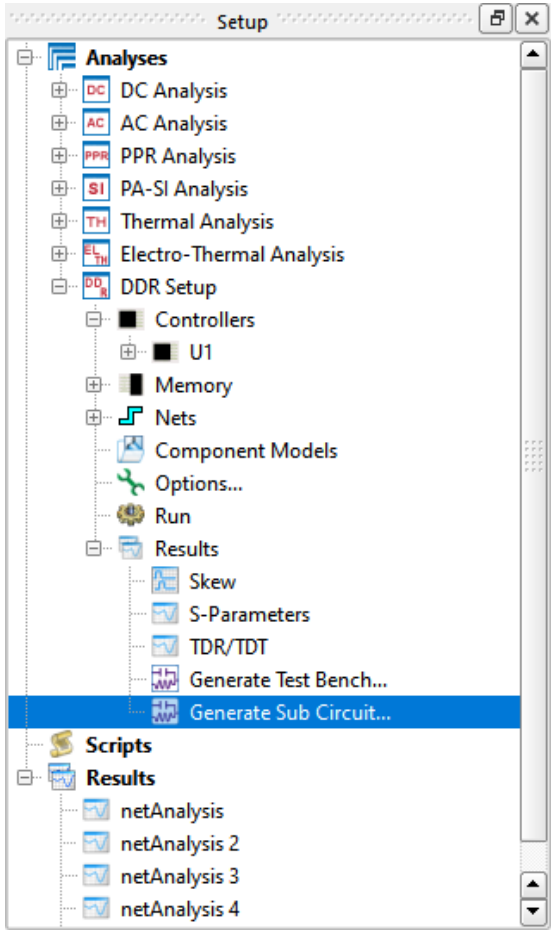
Run Simulation



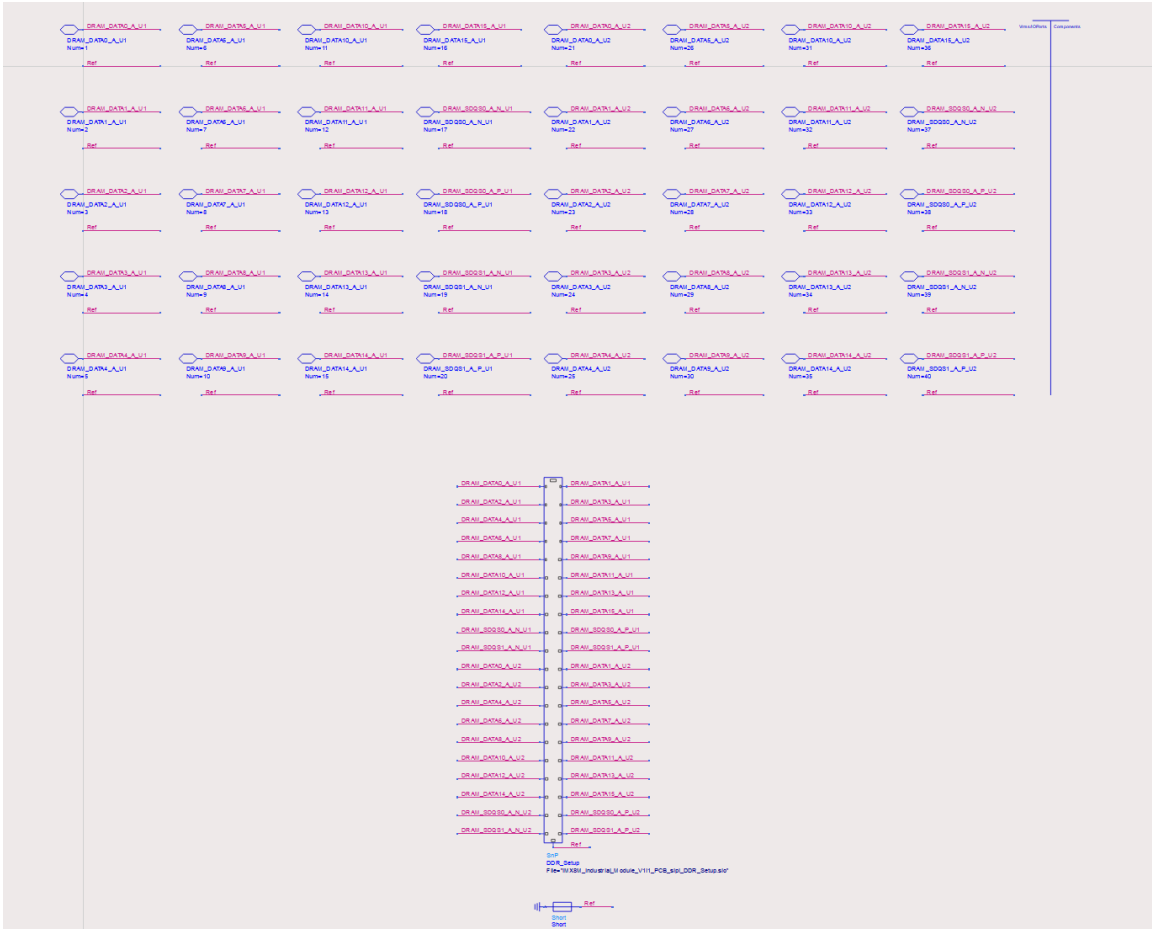
Analyze SIPro DDR Analysis Results

END GOAL: OBSERVE THE EYE RESULTS

- View the results:
  - S-Param insertion loss
  - Skew
  - Utilize sub-circuit to generate info for Memory Designer



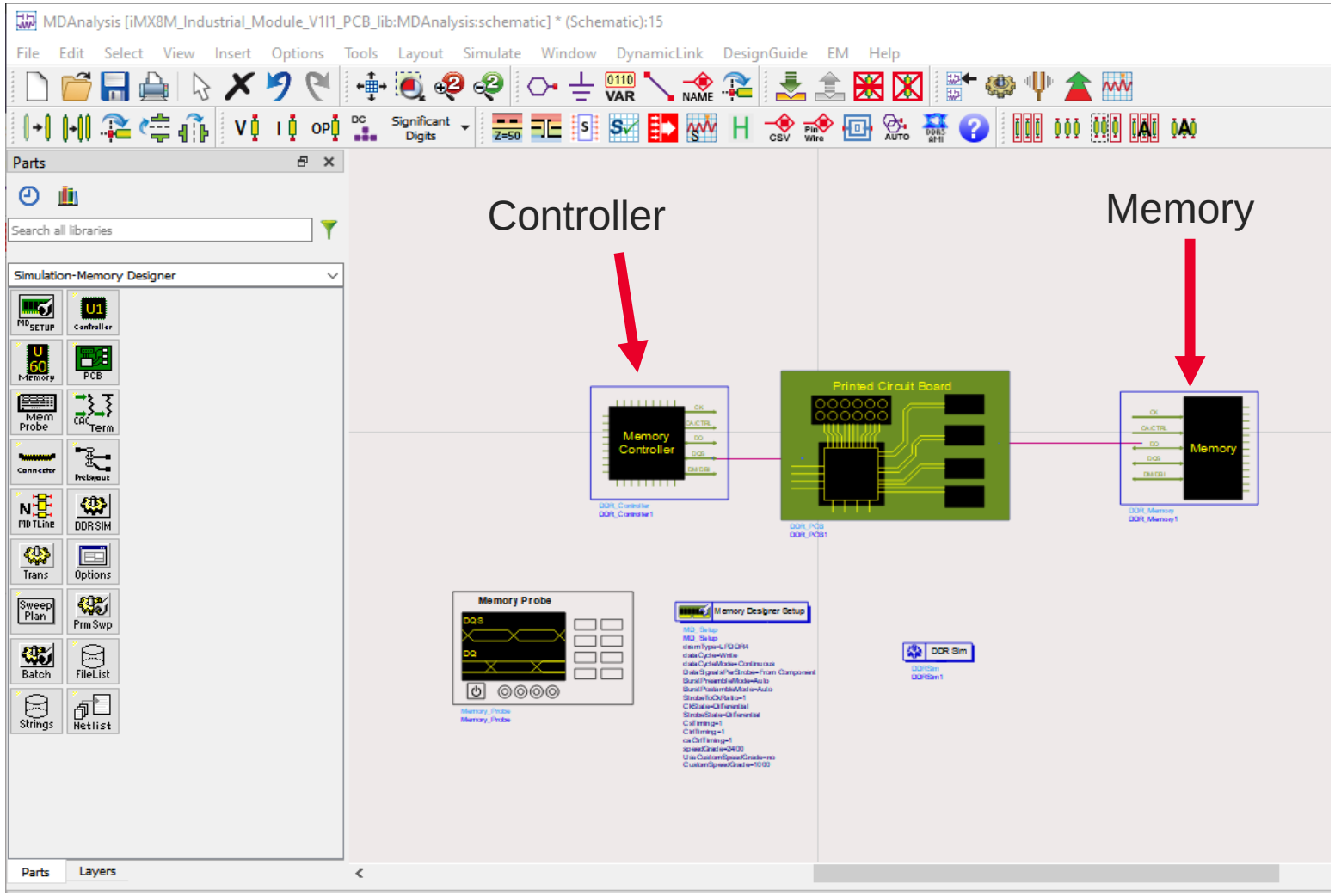
Sub-Circuit Generated:

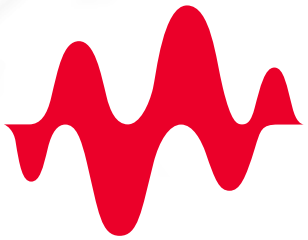


Overview for Today

END GOAL: OBSERVE THE EYE RESULTS

- Memory Designer Setup
- DDR Sim – Which Simulator??
  - Statistical: Takes in ibis analog models(.ibs), good for DDR4 msmts
  - Bit-by-bit: Equalization for Rx model, and IBIS-AMI models, good for DDR5 / LPDDR5
  - Transient Convolution: Takes in S-parameter models to convolve them, giving you waveforms





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