Design & Troubleshooting Tips For Your Switching Regulator

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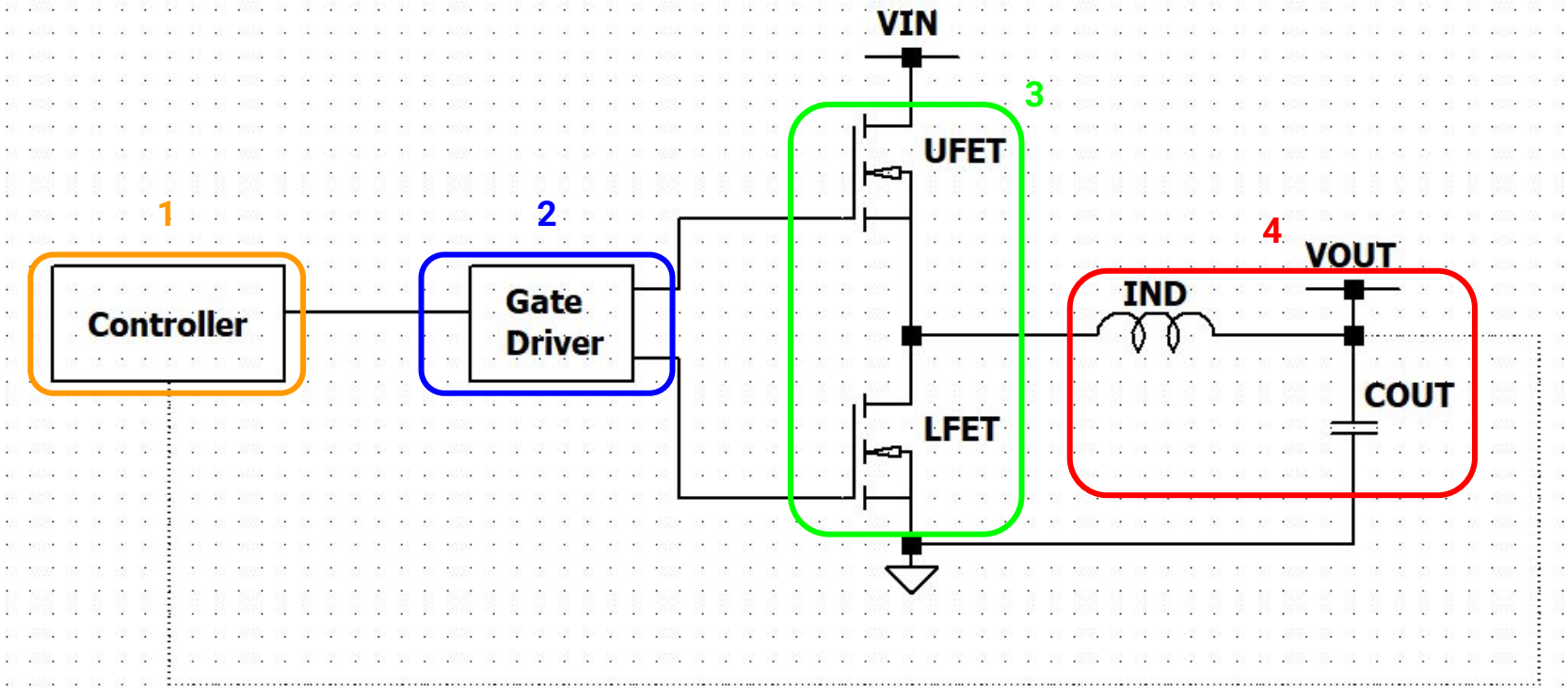
About Me

- Been in the semiconductor industry for over 10 years now as a Systems and Applications Engineer
  - Unlike a Field Application Engineer I go a mile deep but an inch wide
- Worked primarily on multiphase switching regulators for V_{CORE} applications
  - Think power to CPUs, FPGAs, ASICs
- Have seen my parts go into laptops, tablets, phones, servers, and super-computers
- Previously hosted The Engineering Commons Podcast from 2013 to 2018
  - Past guest on The Amp Hour & Embedded.fm podcasts

Main Pieces of a Buck Regulator



Pros & Cons of Integration Levels [Generally]

	All Discrete ICs	Controller + Gate Driver	Gate Driver + FETs [DrMOS]	Controller + Gate Drive + FETs	Module [All + Passives]
Price	Low to Medium	Low to Medium	Medium to High	Medium to High	High
PCB Area	High	High	Medium	Low	Low
Component Count	High	High	Medium	Low	Low
Design Flexibility	High	High	Medium	Low	Low
Design Complexity	High	High	Medium	Low	Low

Component Selection – Control Scheme

- Can quickly fall down a rabbit hole studying all possible options out there
- Boils down to two main schemes
  - Voltage Mode Control
    - Simple to implement
    - Single control loop
    - LC double pole tricky to compensate
    - Poor regulation with changing V_{IN}
  - [Peak] Current Mode Control
    - Eliminates LC double pole for simpler compensation
    - Requires addition of slope compensation
    - Better line transient response
    - Proper current sense implementation is critical

Component Selection - Inductor

Core Material

- Ferrite
  - Hard Saturation
  - Lower DCR
- Composite
  - Soft Saturation
  - Higher DCR

Physical Size & Value

- Don’t forget the Z-axis
  - Thicker chokes typically have better core loss
- Inductance Value
  - Trade off between efficiency, ripple, and transient response

Placement

- Short, wide, trace from SW node to inductor
- Keep on same layer as FETs
  - Minimize critical loop
- If marked, put dotted sided to SW node for better EMI

Component Selection – Capacitors

Bulk Capacitors

- ESR Zero has to be accounted for during compensation
- ESR can be used to dampen acoustic noise under the right circumstances

All Ceramic C_{OUT}

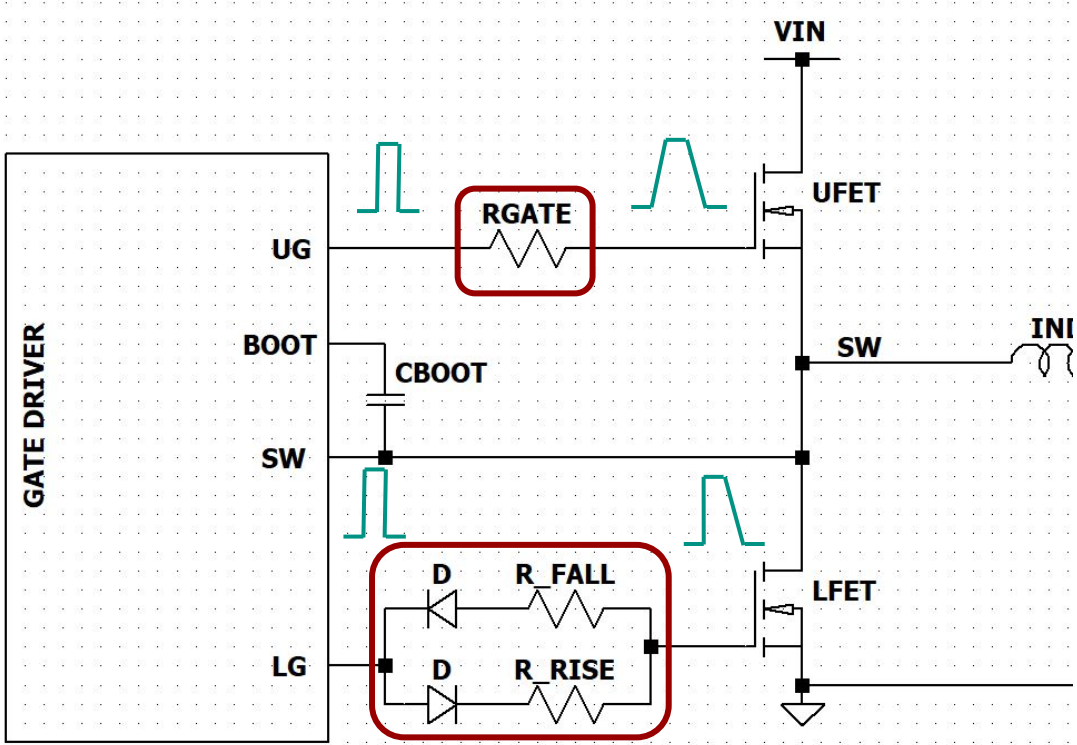
- Some control schemes DON'T support this
  - Early V^2 control
  - Read Datasheet Carefully

Input Ceramics

- Don't forget to account for derating!
  - C drops with DC bias
- Size capacitance for DC ripple voltage
- # of caps for input ripple current

Placement is critical!

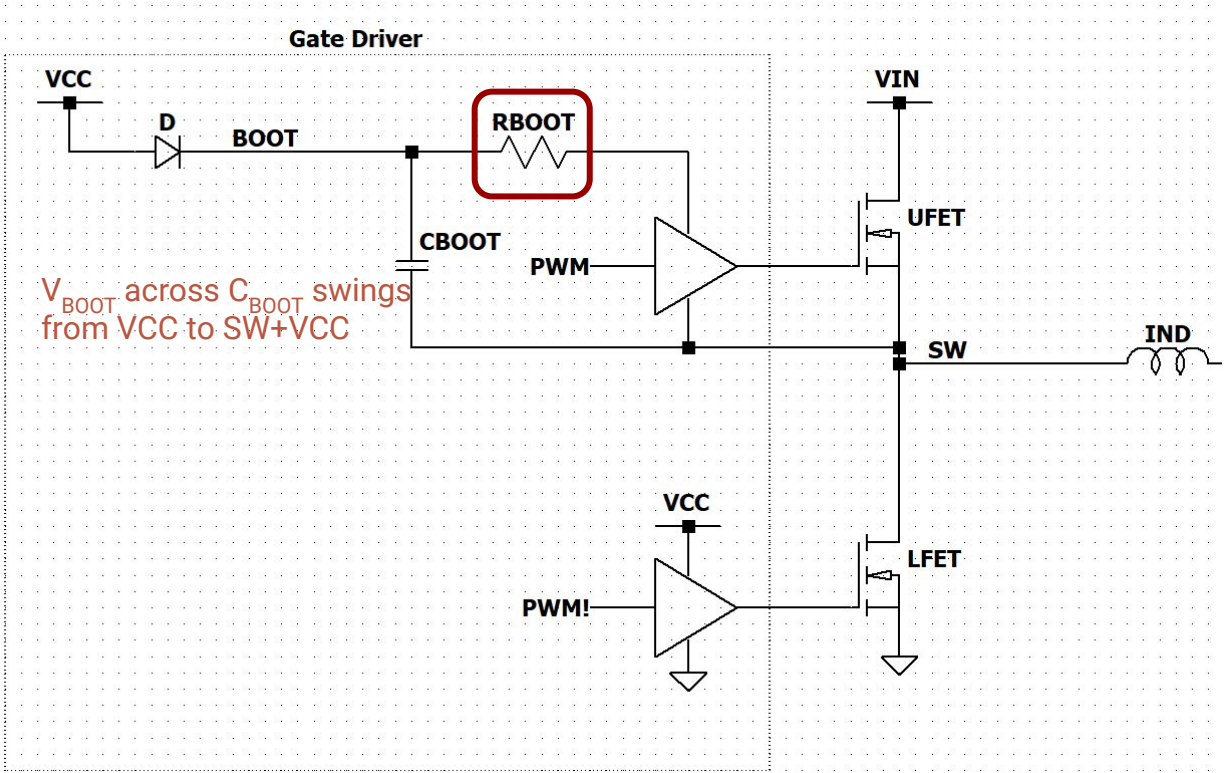
Debugging Hooks - Gate Resistors



Gate Resistor

- Controls turn on/off slew of the power FETs
- Single Resistor
  - Cheap
  - Equally affected Rise & Fall edges
- Resistor + Diodes
  - Extra Cost & Area
  - Independent Rise & Fall Control
- Can hurt efficiency or cause shoot-through if done incorrectly

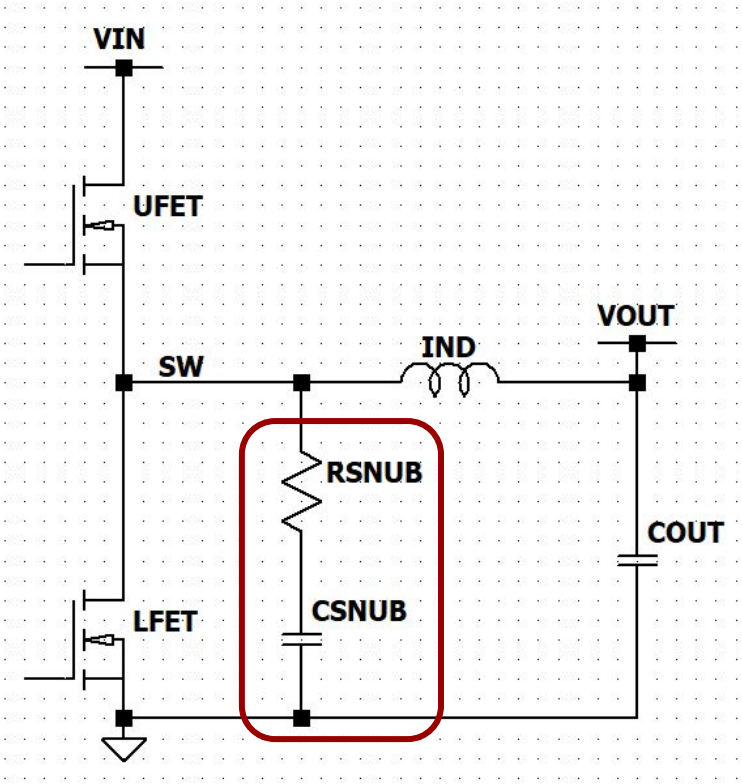
Debugging Hooks – Boot Resistor



Boot Resistor

- Limits the current to the upper FET gate driver slowing down SW node rise time
- Can help reduce shoot-through or EMI
- Start with small value!
  - ~1Ω Typically
- Place R_{BOOT} & C_{BOOT} close to Gate Driver on PCB

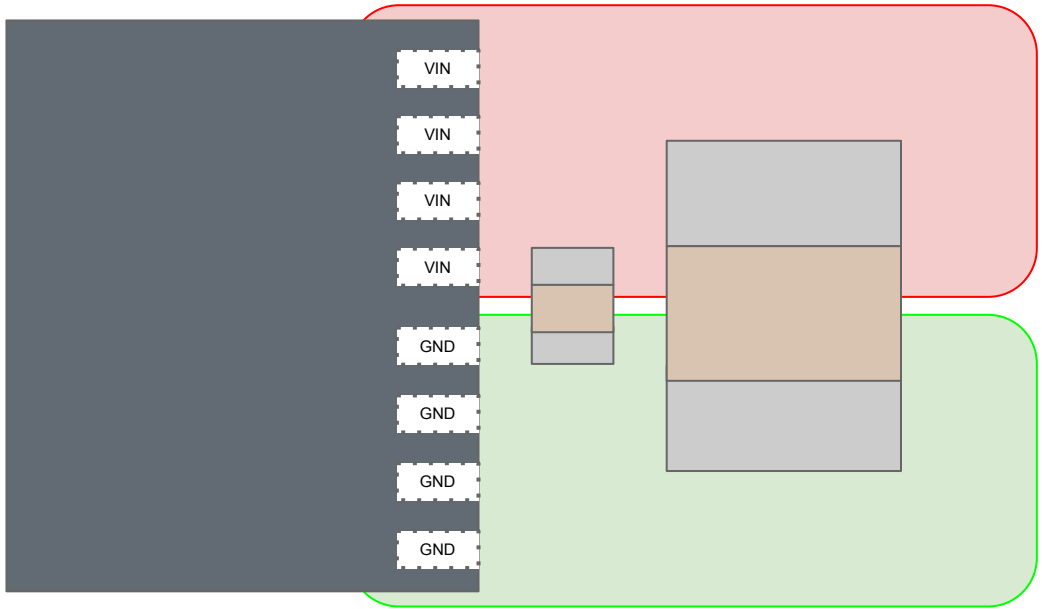
Debugging Hooks – Phase Snubber



Phase Snubber

- Keep as DNP to start
  - Populate if you run into trouble
- Reduces ringing on the SW node
  - Keep FETs within datasheet limits
  - Lower EMI
- Secondary layout concern after FETs/Ind/C_{IN}/C_{OUT}

Debugging Hooks – VIN MLCC



- Sneak in small package MLCC as close to VIN/GND on the FETs as possible
  - Can leave DNP to start if BOM cost is an issue
- Can reduce ringing on the switch node
  - Lowers EMI
  - Better device reliability if exceeded datasheet limits
- Doesn’t replace good design/layout practices

Validation Tips – Probing Techniques

Tight GND Connection

- Avoid using the long ground clip whenever possible
  - Keep ground connection close to signal of interest
- Long leads can show false failures
  - Ringing
  - V_{OUT} Ripple

Differential Probe

- Don't exceed the common mode range!
  - SW Node
  - BOOT-SW
  - V_{IN}
  - Upper Gate Drive
- When measuring ripple and other low-level signals be aware of the diff probe noise floor

DIY Power Rail Probe

- Low cost, low noise
- Cleanest signal when used correctly

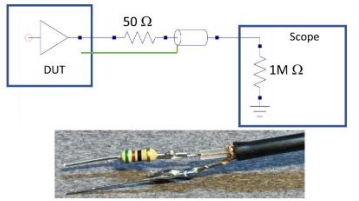
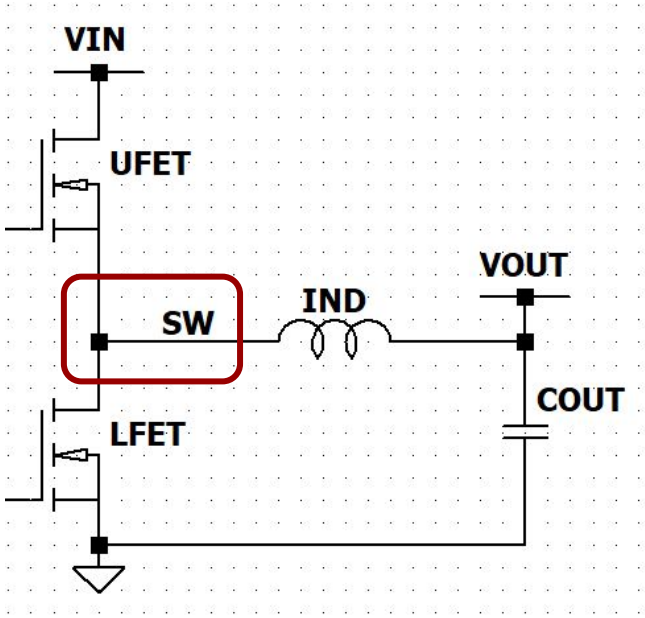


Figure 1: The source series termination method presents an alternative method of probing low-impedance, fast-switching sources

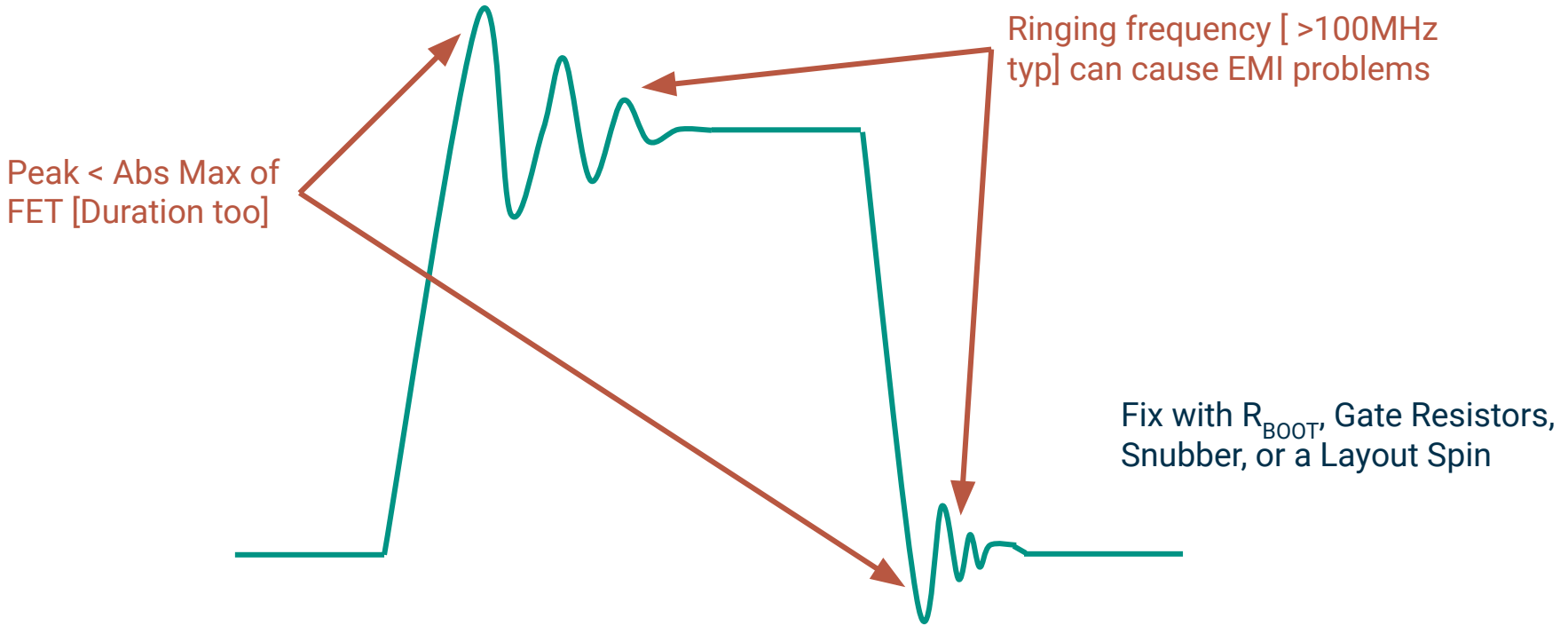
Source: Teledyne LeCroy

Validation Tips - The Importance of Phase

- The switch node is definitely one of the most critical nodes of a regulator
- It can tell you a lot about the health of your system
  - EMI
  - Efficiency/Reliability
  - Stability/Jitter

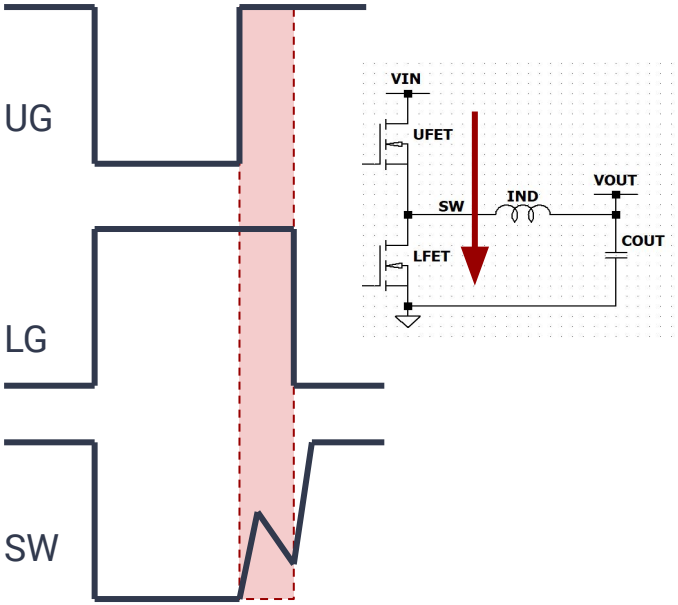


The Importance of Phase – EMI

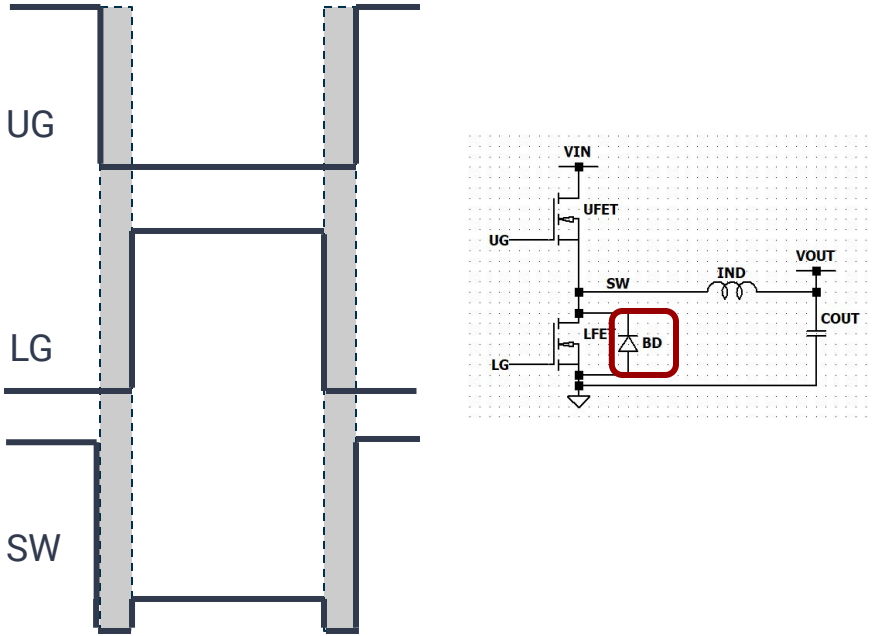


Importance of Phase – Efficiency/Reliability

Shoot-Through

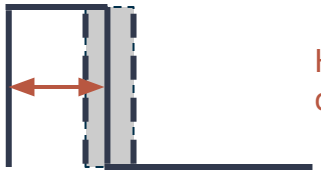


Dead Time



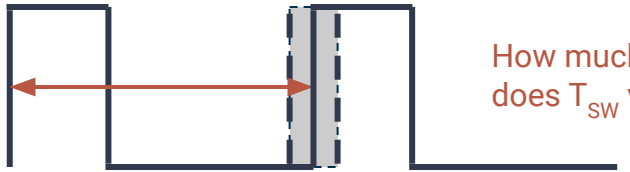
Importance of Phase – Stability/Jitter

Edge Jitter



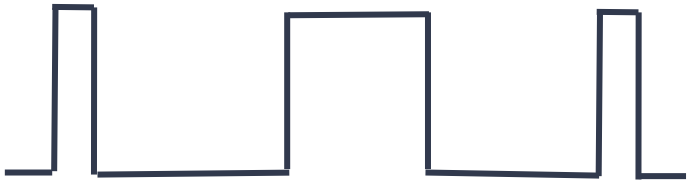
How much does T_{ON} vary?

Period Jitter



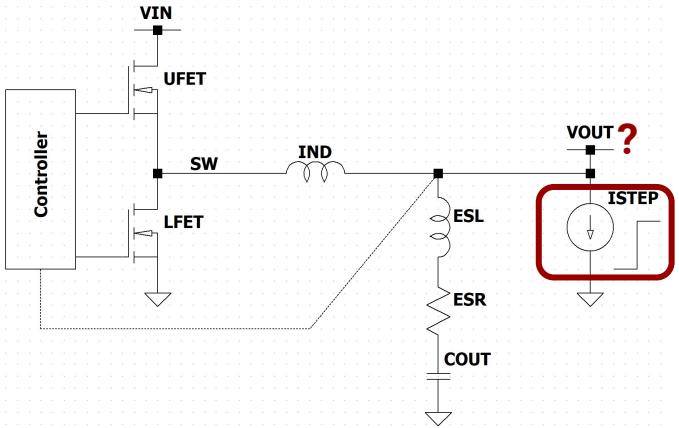
How much does T_{SW} vary?

Stability



Alternating Narrow & Wide Pulses is a sign of poor Gain Margin & a Compensation problem

Validation Tips – Transient Testing



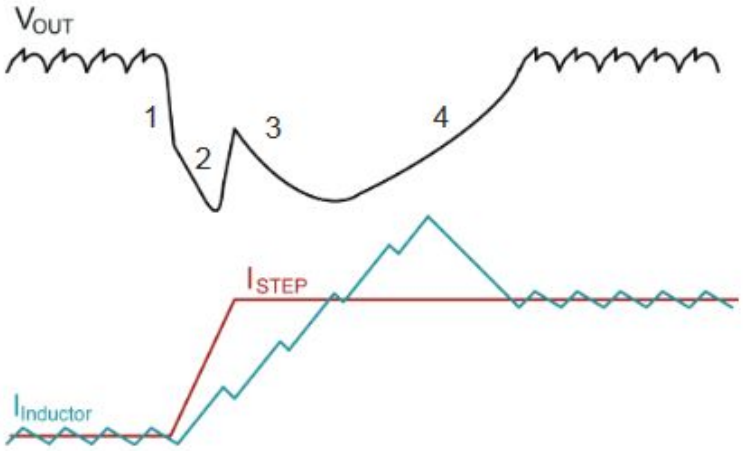


Figure 5 – Transient response in the time domain.

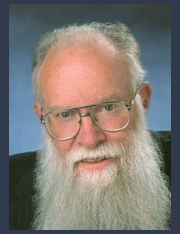
Source: [Texas Instruments SLUP391]

Region 1 - ESL Spike, Faster Slew → Larger Spike
Region 2 - ESR Droop, Inductor Current starts to slew
Region 3 - C_{OUT} Discharges to maintain V_{OUT}
Region 4 - Inductor Current = Load Current, overshoots to refill COUT

Reading the Datasheet

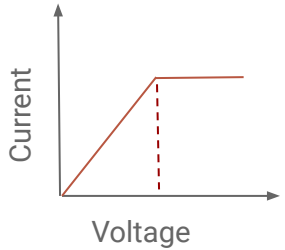
- They all could be better [trust me] but in most cases they’re not a bad document for how the regulator operates at a high level
  - Check for app notes, design guides, white papers, etc. for more info as needed
- Know when to deviate!
  - Check the Typical Applications listed & Reference Circuits against your design
  - Compare the Layout Guidelines against your PCB
- Skim through first before reading in more detail
  - Call out relevant tables, figures, and graphs to reference later
  - If a spec on Page 1 is critical to your design find every mention of it in the document to make sure it’s true

Floobydust

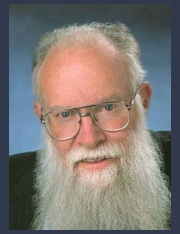


Source: Wikipedia

- Fault Response is an often overlooked, don't let it bite you
  - Latched or Hiccup?
  - OVP, OCP → Tri-state SW or Pull Low?
  - OCP → Peak, Valley, or Average Limit?
- Electronic Loads are incredibly useful but come with gotchas of their own
  - Slow slew rates and long cables make it hard to really test transient response
  - Cable inductance can make V_{OUT} ring below ground as regulator turns off for whatever reason
  - Know the minimum V_{OUT} that can pull the max load



Floobydust Continued



Source: Wikipedia

- An IR camera is invaluable to have on hand if you can swing it
  - See where current is flowing after a load is applied by watching what heats up first
  - Find minor shorts that don't result in shutdown
- Improve a heat sink by placing hex nuts on top of your FETs [carefully]
- Troubleshooting Mindset
  - Start simple - Power, Jumper/Switch positions, Probe Location, etc.
  - Visual checks are perfectly valid and can save a ton of time
- Best way to learn
  - Torture a cheap eval board or make your own
  - Read/watch whatever interests you and branch out from there
  - Be okay with the unknown, you'll figure it out eventually

Helpful Resources

- Linear Circuit Design Handbook - Chapter 9, Analog Devices
- Reducing Buck Converter EMI - Texas Instruments
- TI Power Supply Design Seminar - Texas Instruments [needs TI account]
- Under the Hood of Low Voltage DC/DC Converters - Texas Instruments
- Ridley Design Center - Ridley Engineering
- Linear Tech AN149 - Analog Devices
- Snubber Design - Rohm
- Power MOSFET Basics - Infineon
- Avoiding Parasitic Turn On - Infineon
- Electrical Integrity - Istvan Novak
- Multiphase 101 Training Portal - Texas Instruments
- Biricha YouTube Channel
- Ridley Engineering YouTube Channel
- Control Mode Quick Reference Guide - Texas Instruments
- PCB Layout Considerations for Non-Isolated Switching Power Supplies - Analog Devices